

# Christopher W. Fletcher

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CONTACT	<i>E-mail:</i> cwfletch@mit.edu <i>Website:</i> <a href="http://cwfletcher.net">http://cwfletcher.net</a> <i>Last updated:</i> April, 2012
AFFILIATION	Massachusetts Institute of Technology Computer Science and Artificial Intelligence Lab (CSAIL)
ADDRESS	Ray and Maria Stata Center, 32-G884 32 Vassar Street, Cambridge, Massachusetts
EDUCATION	<b>Massachusetts Institute of Technology</b> <b>Aug 2010 - Present</b> M.S./Ph.D., Electrical Engineering and Computer Science, candidate Advisor: Srimi Devadas <b>The University of California, Berkeley</b> <b>Aug 2006 - May 2010</b> B.S., Electrical Engineering and Computer Science Advisor: John Wawrzynek <b>Viewpoint School, Calabasas</b> <b>Aug 1994 - Jun 2006</b> {Elementary, High} School Diplomas
RESEARCH	1. Research Assistant <b>Fall 2010 - Present</b> Affiliation: <i>MIT; CSAIL; Computation Structures Group</i> Advisor(s): Srimi Devadas 2. Undergraduate Researcher <b>Spring 2008 - Spring 2010</b> Affiliation: <i>U.C. Berkeley; BWRC, ParLab; RAMP, Berkeley Reconfigurable Group</i> Advisor(s): John Wawrzynek, Garry Nolan, Greg Gibeling, Narges Asadi
TEACHING	<b>CS61A:</b> Structure and Interpretation of Computer Programs, U.C. Berkeley <b>CS150:</b> Components and Design Techniques for Digital Systems, U.C. Berkeley <b>6.S092:</b> Introduction to Software Engineering in Java (IAP), M.I.T. 1. Instructor <b>Spring 2012</b> <i>6.S092</i> ; with: Anirudh Sivaraman and Kasia Hayden 2. Teaching Assistant (Rating: 5/5) <b>Spring 2010</b> <i>CS150</i> ; under: John Wawrzynek 3. Teaching Assistant (Rating: 4.7/5) <b>Spring 2009</b> <i>CS150</i> ; under: John Wawrzynek 4. Head Teaching Assistant (Rating: 4.8/5) <b>Fall 2008</b> <i>CS150</i> ; under: Kris Pister 5. Grader <b>Fall 2007</b> <i>CS61A</i> ; under: Brian Harvey 6. Lab Assistant <b>Spring 2007</b> <i>CS61A</i> ; under: Brian Harvey
INDUSTRY	1. Software Engineering Intern <b>Sum 2008</b> <i>Oracle Corporation</i> ; Project: JDeveloper-JIRA Connector

VOLUNTEER	1. Corporate Liaison Committee Chair <i>The Engineers' Joint Council</i>	<b>2006 - 2008</b>
	2. Mentor, Media Literacy Program Director <i>The Zeitgeist Community Learning Center</i>	<b>2005 - 2007</b>
	3. School Representative, Organizer <i>The ALS Association - Greater Los Angeles Chapter</i>	<b>2005 - 2006</b>
AWARDS	National Defense Science and Engineering Graduate Fellowship	<b>Funding years: 2012-2015</b>
	National Science Foundation Graduate Research Fellowship	<b>Funding years: 2011</b>
	ICS'10 Conference Best Student Paper Award	<b>2010</b>
	U.C. Berkeley, graduated with <i>High Honors</i> (GPA: 3.91/4)	<b>2010</b>
	Rose Hills Science and Engineering Scholarship	<b>2007-2008</b>
	UC Berkeley Edward Frank Kraft Scholarship	<b>2006</b>
VSSA Award (Community Service Distinction)	<b>2006</b>	
AFFILIATIONS	Golden Key	<b>2008</b>
	Tau Beta Pi	<b>2007</b>
	Eta Kappa Nu (invited)	<b>2007</b>
	National Society of Collegiate Scholars	<b>2006</b>
	Cum Laude Society, Honor Society	<b>2006</b>
	CORE, Community Service Honor Society	<b>2005</b>
JOURNAL PAPERS	1. P. Ren, M. Lis, M. H. Cho, K. S. Shim, <b>C. W. Fletcher</b> , O. Khan, N. Zheng, and S. Devadas. "HORNET: a cycle-level multicore simulator". <i>To appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)</i> , 2012.	
	2. I. Lebedev, <b>C. W. Fletcher</b> , S. Cheng, J. Martin, A. Douppnik, D. Burke, M. Lin, and J. Wawrzynek. "Exploring Many-core Design Templates for FPGAs and ASICs". <i>Appears in the International Journal of Reconfigurable Computing (IJRC)</i> , 2011. <b>Invited Paper, peer reviewed.</b>	
CONFERENCE PAPERS	1. M. Lis, P. Ren, M. H. Cho, K. S. Shim, <b>C. W. Fletcher</b> , O. Khan, and S. Devadas. "Scalable Accurate Multicore Simulation in the 1000 core era". <i>Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)</i> , 2011.	
	2. <b>C. W. Fletcher</b> , I. Lebedev, N. B. Asadi, D. Burke, J. Wawrzynek. "Bridging the GPGPU-FPGA Efficiency Gap". <i>Proceedings of the 19th International Symposium on Field-Programmable Gate Arrays as a short paper (ISFPGA)</i> , 2011.	
	3. I. Lebedev, S. Cheng, A. Douppnik, J. Martin, <b>C. W. Fletcher</b> , D. Burke, M. Lin, J. Wawrzynek. "MARC: A Many-Core Approach to Reconfigurable Computing". <i>Proceedings of the 6th International Conference on Reconfigurable Computing and FPGAs (ReConFig)</i> , 2010.	
	4. N. B. Asadi*, <b>C. W. Fletcher</b> *, G. Gibelg, E. N. Glass, K. Sachs, D. Burke, Z. Zhou, J. Wawrzynek, W. H. Wong, and G. P. Nolan. "ParaLearn: A massively parallel, scalable system for learning interaction networks on FPGAs". <i>Proceedings of the 24th International Conference on Supercomputing (ICS)</i> , 2010. <b>Best Student Paper Award.</b>	
	*: Co-lead authors.	
ABSTRACTS	1. M. Lis, K. S. Shim, M. H. Cho, <b>C. W. Fletcher</b> , M. Kinsy, I. Lebedev, O. Khan, and S. Devadas. "Brief Announcement: Distributed Shared Memory based on Computation Migration". <i>Proceedings of the 23rd Symposium on Parallelism in Algorithms and Architectures (SPAA)</i> , 2011.	
TECH REPORTS	1. <b>C. Fletcher</b> , M. V. Dijk, and S. Devadas. "Compilation Techniques for Efficient Encrypted Computation". <i>Cryptology ePrint Archive (IACR)</i> , Report 2012/266, 2012.	

## TALKS

1. Bridging the GPGPU-FPGA Efficiency Gap.  
*“FPGA Architectures and Technology” Technical Session at the 19th Intl. Sym. on FPGAs*, Monterey, California (2/28/2011)
2. ParaLearn: A massively parallel, scalable system for learning interaction networks on FPGAs.  
*“Applications” Technical Session at the 24th Intl. Conf. on Supercomputing*, Tsukuba, Japan (6/2/2010)
3. Scalable Bayesian Network Discovery with Reconfigurable Hardware.  
*RAMP Winter Retreat*, U.C. Santa Cruz (1/28/2010)  
*BWRC Winter Retreat*, Lake Tahoe (1/10/2010)
4. Reconfigurable Computing & Bayesian Networks.  
*GSRC Annual Research Symposium*, San Jose (9/3/2009)
5. Introduction to GateLib & MCMC on the BEE3.  
*Nolan Lab “All Hands Meeting”*, Stanford (6/15/2009)

## POSTERS

1. Bridging the GPGPU-FPGA Efficiency Gap.  
*International Symposium on Field-Programmable Gate Arrays*, Monterey (2/28/2011)
2. Scalable FPGA Solutions for Learning Bayesian Networks.  
*BWRC Summer Retreat*, U.C. Berkeley (6/6/2010)  
*BWRC Winter Retreat*, Lake Tahoe (1/10/2010)
3. Curing Cancer with RCBIOS.  
*RAMP Summer Retreat*, U. T. Austin (6/23/2009)
4. flint.  
*RAMP Winter Retreat*, U.C. Berkeley (1/10/2009)

COURSEWORK  
(MIT)

User Interface Design (6.831)	2012
Machine Learning (6.867)	2011
Statistical Learning Theory and Applications (9.520)	2011
Introduction to the Theory of Computation (6.840)	2010
Foundations of Program Analysis (6.820)	2010

COURSEWORK  
(BERKELEY)

Introduction to Artificial Intelligence (CS188)	2010
VLSI Systems Design (CS250)	2009
Programming Languages and Compilers (CS164)	2009
Hardware Design Patterns (CS294-48)	2009
Efficient Algorithms and Intractable Problems (CS170)	2009
Operating Systems and System Programming (CS162)	2009
Computer Architecture and Engineering (CS152)	2009
“Capstone” Digital Design Laboratory (CS194-6)	2008
Signals and Systems (EE20)	2008
Introduction to Microelectronic Circuits (EE40)	2008
Components and Design Techniques for Digital Systems (CS150)	2008
Discrete Math and Probability (CS70)	2008
Machine Structures (CS61C)	2007
Data Structures and Programming Methodology (CS61B)	2007
Web 2.0 Programming Using Ruby on Rails (CS98)	2007
The Structure and Interpretation of Computer Programs (CS61A)	2006

## KNOW-HOW

**Languages:** A bunch of functional/scripting/imperative/object-oriented/hardware-description/assembly languages (I have less experience with constraint/web programming and am currently learning more about parallel languages)

**EDA:** ModelSim, Xilinx ISE (ChipScope, FPGA Editor, Floorplanner, CoreGen, etc), Synopsys {Synplify Pro, {DC, IC} Compiler, Formality, PrimeTime}